TAIWAN SEMICONDUCTOR

# AN-1004

# Soldering Optimization For PDFN1012 Package

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# Soldering Optimization For PDFN1012 Package

## Introduction

Taiwan Semiconductor's innovative new PDFN1012 dual MOSFET package offers several advantages to the engineer working to improve SMPS and load switching power density and performance. The PDFN1012 integrates two high power MOSFET die into a small thermally efficient footprint. The small, thin, leadless package is optimized for today's high throughput surface mount pick and place and reflow soldering processes.

This document provides the results of solder paste application experiments designed to study the effects of solder paste patterns on resultant solder voids after IR reflow. Solder patterning guidelines to reduce voiding are given.

## PDFN1012 package description

Figure 1 highlights the PDFN1012 package configuration. Taiwan Semiconductor is the first to offer this high power-density package. The first products offered in this package are dual 600V, low $R_{DS(ON)}$ high performance super junction MOSFETs applicable to various SMPS topologies such as interleaved or bridgeless PFC .

The small and efficient construction of this package offers low parasitic inductance in the package and to reduce switching spikes and EMI. The mirrored gate pin allocation is also very helpful for PCB layout and to decrease noise interference.

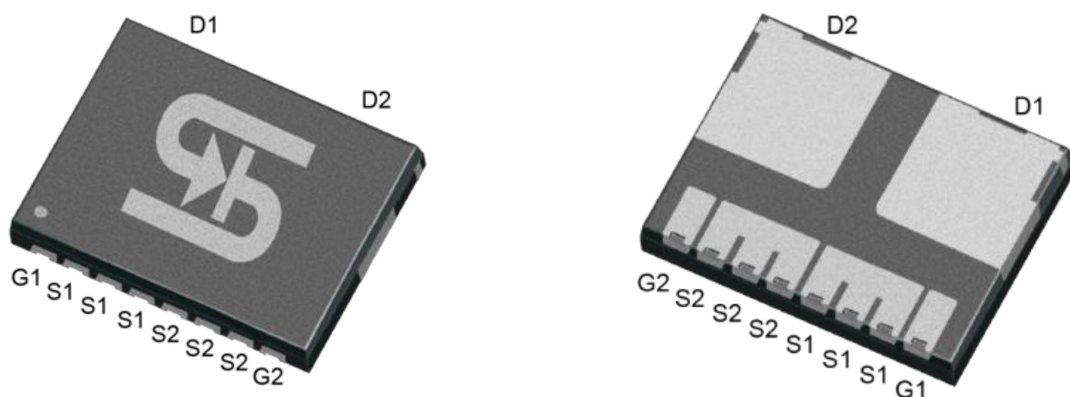



**Figure 1. PDFN1012 Package (Top and Bottom View**)

Figures 2 and 3 show the PDFN1012 dimensioned package drawing and recommended PCB land pattern design. PCB land pattern and solder mask design along with the design of the solder screen thickness and openings is very important to reliable soldering process and solder void minimization. Solder voids increase the thermal impedance between the package and the ambient environment and reduce the thermal efficiency of the system.

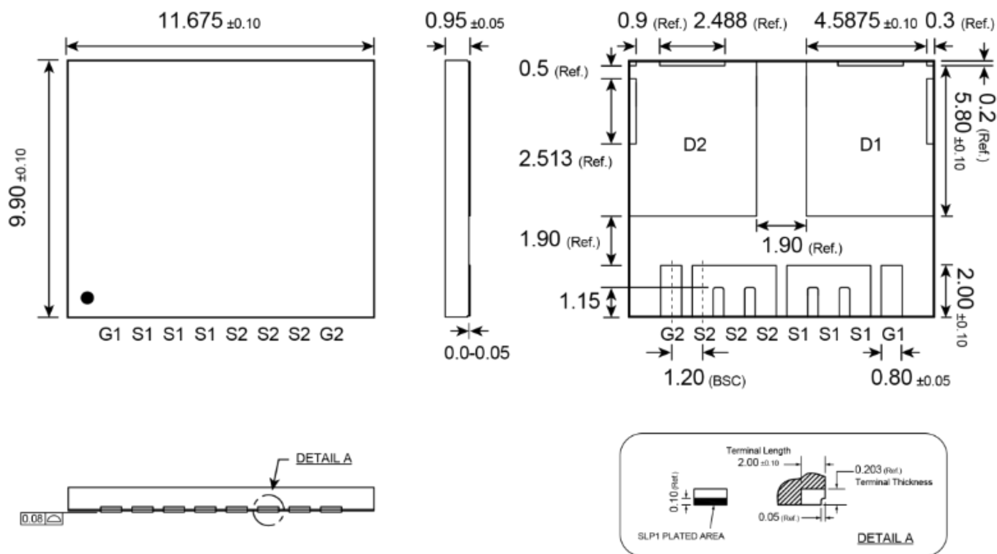



**Figure 2. PDFN1012 Package dimensions**

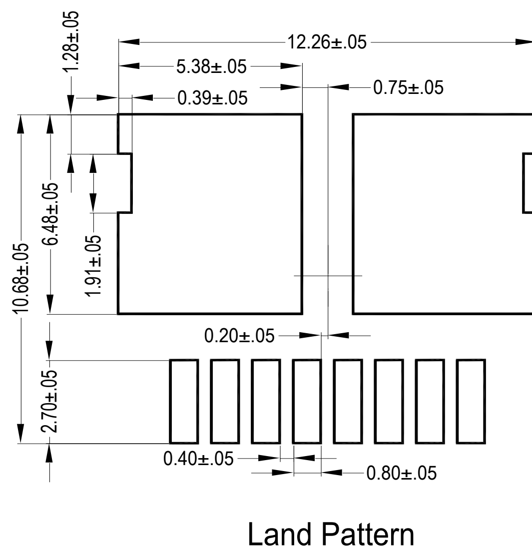



**Figure 3. PDFN1012 Package dimensions and recommended PCB land pattern.**

## PDFN1012 solderability enhancement

Solder joint integrity for any surface mount component depends on many factors including PCB land pattern, PCB layer structure, copper thickness, layout position on the PCB, solder paste and flux chemistry, solder paste stencil design and thickness, and IR reflow profile. The component package design also significantly affects the solderability and solder joint integrity in application. Component pin design and resultant solder fillet following reflow is one the key factors that determines solder joint integrity and long term reliability.

The Taiwan Semiconductor PDFN1012 package was designed with a “natural fillet” design structure to ensure that a robust solder fillet results upon reflow. Figure 4 illustrates this “natural fillet” design concept.

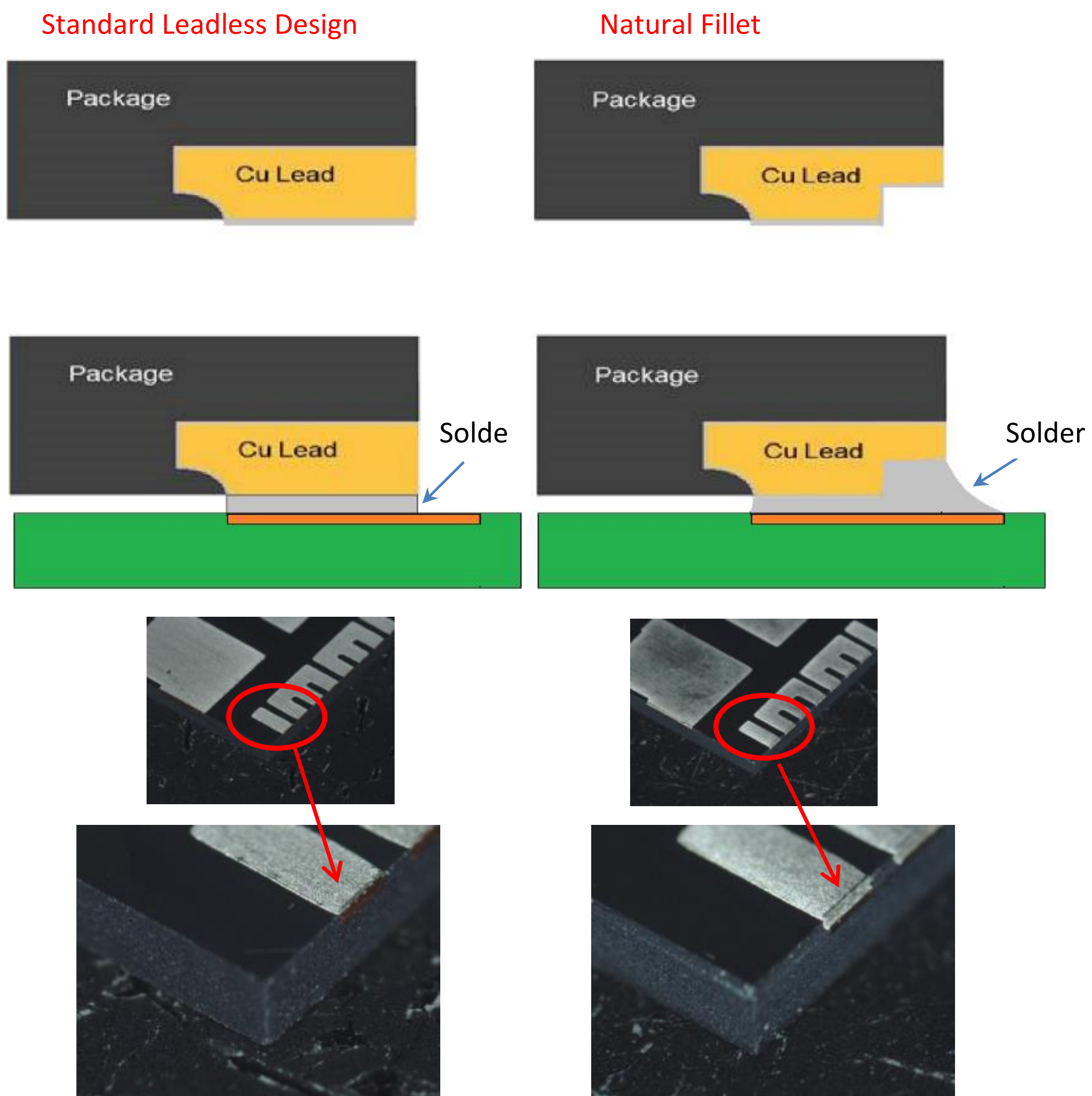



**Figure 4. PDN1012 Natural Fillet design structure**

Figure 5 shows the larger solder contact area and solder volume using the natural fillet structure.

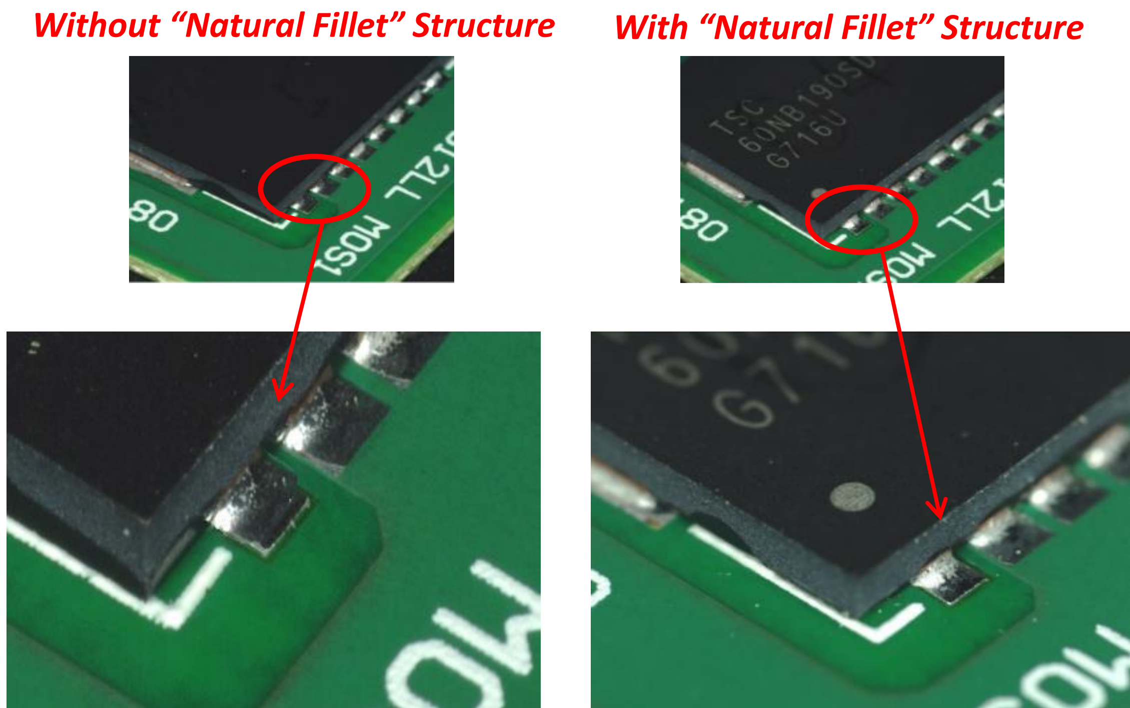



**Figure 5. PDN1012 Solder volume comparison with and without the Natural Fillet design structure**

Figure 6 shows a cross-sectional comparison highlighting improved and robust solder fillet contact.

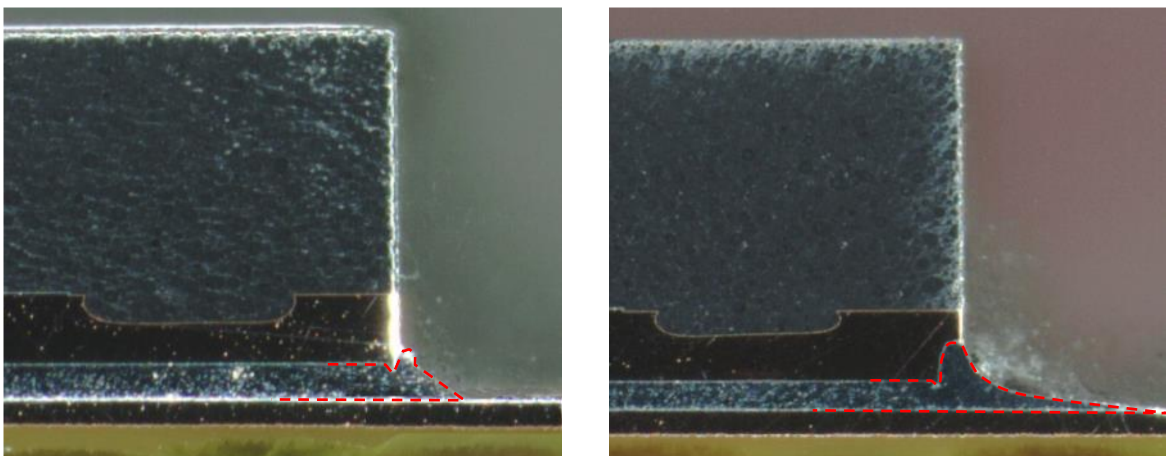


**Figure 6. PDN1012 Solder fillet comparison with and without the Natural Fillet design structure**

## Solder paste

Solder alloys and flux components contribute to the solderability of the component and the voiding generated under power package thermal relief structures. To meet worldwide and European environmental RoHS requirements,

TSC used M705 lead (Pb)-free solder paste (Sn 96.5%/Ag 3.0%/Cu 0.5%) which is lead-free, water-soluble, and no-clean for this solderability study. M705 was the only solder paste used during these experiments.

## Reflow profile

An optimized reflow profile is critical to component solderability and reliability. An optimal reflow profile for any given application will depend on the several factors including solder paste chemistry, oven type, PCB material and construction, and reflow component types.

Solder quality problems such as solder balling, cold solder joints, and solder voiding are indicators that the solder reflow profile is not optimized for the circuit board assembly.

Figure 7 shows the multizone IR reflow oven used and the reflow profile programmed for the circuit board assemblies during this study. The profile follows IPC/JEDEC J-STD-020 guidelines for lead free processes.

**Figure 7. Multi zone IR oven and reflow profile for PCB assemblies using M705 Pb-free solder paste**

## Stencil aperture design variations

The key variable tested during this study was the solder stencil aperture geometry. Stencil thickness was constant at 0.12mm. Stencil aperture pattern and geometry variations were evaluated for their effect on solder coverage, solder void generation, and post reflow coplanarity.

IPC-7525 stencil design guidelines for solder paste coverage (50 to 80% of land area) and acceptable solder paste release (>1.5 solder paste aspect ratio and >0.66 solder-paste to land-area ratio) were used. Solder paste aperture patterns included circular and rectangle arrays of different dimensions and sizes. Figure 8 and Table 1 highlight the stencil design parameters used in this study.

Figures 10 – 17 detail each stencil aperture design. Figure 18 show a PCB with the resultant solder paste layer after solder paste screening and reflow process.

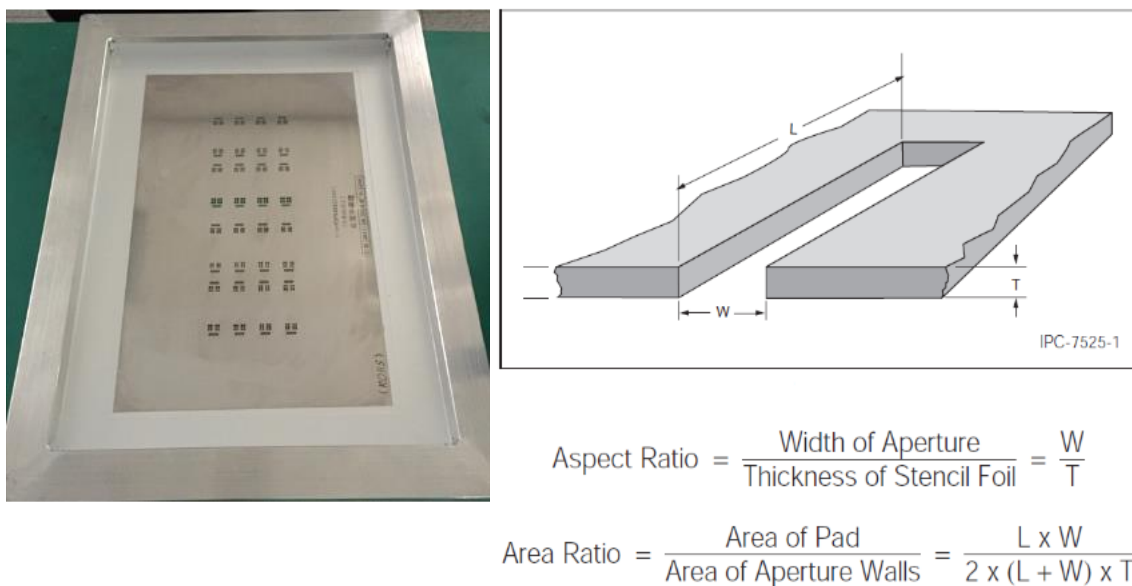



**Figure 8. Overview of solder stencil and cross sectional view of a stencil aperture**

According to different stencil aperture structure conditions for PDFN1012 solder void free evaluation. The purpose is looking for which one is optimization for solder void free less.

**Table 1. Stencil aperture descriptions**

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1.49 | 1.94 | 0.50 | 0.50 | 0.12 | 3 | 2 | 50.9% | 34.12 | 5.38 | 6.48 |
| 2 | 1.36 | 1.79 | 0.60 | 0.60 | 0.12 | 3 | 2 | 42.8% | 34.12 | 5.38 | 6.48 |
| 3 | 1.23 | 1.64 | 0.70 | 0.70 | 0.12 | 3 | 2 | 35.4% | 34.12 | 5.38 | 6.48 |
| 4 | 1.63 | 1.26 | 0.40 | 0.40 | 0.12 | 3 | 3 | 54.1% | 34.12 | 5.38 | 6.48 |
| 5 | 2.84 | 2.37 | 0.50 | 0.50 | 0.12 | 2 | 2 | 78.9% | 34.12 | 5.38 | 6.48 |
| 6 | Circular -- 0.5mm x 5pcs / 1.2mm x 4pcs / 1.6mm x 4pcs / 2.0mm x 1pcs | | | | 0.12 | | | 47.9% | 34.12 | 5.38 | 6.48 |
| 7 | Circular -- 0.5mm x 27pcs / 1.3mm x 8pcs | | | | 0.12 | | | 45.7% | 34.12 | 5.38 | 6.48 |
| 8 | 0.93 | 0.97 | 0.30 | 0.30 | 0.12 | 5 | 4 | 51.8% | 34.12 | 5.38 | 6.48 |

There are eight kind of stencil structure for PDFN1012 solder void free solution evaluation. There are different eight stencil opening ratio structures. As following Figure 9

Stencil opening ratio

- No 1 : 50.9%
- No 2 : 42.8%
- No 3 : 35.4%
- No 4 : 54.1%
- No 5 : 78.9%
- No 6 : 47.9%
- No 7 : 45.7%
- No 8 : 51.8%

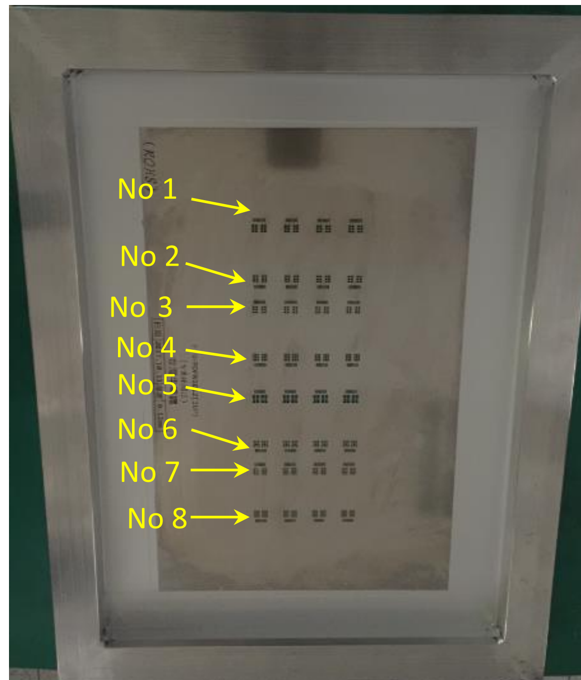



**Figure 9. Stencil opening ratio of the eight aperture types**

Stencil Structure Condition 1 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1.49 | 1.94 | 0.50 | 0.50 | 0.12 | 3 | 2 | 50.9% | 34.12 | 5.38 | 6.48 |

- Type: No 1.
- 6 block rectangles
- Solder ratio: 50.9%
- Stencil thickness is 0.12 mm

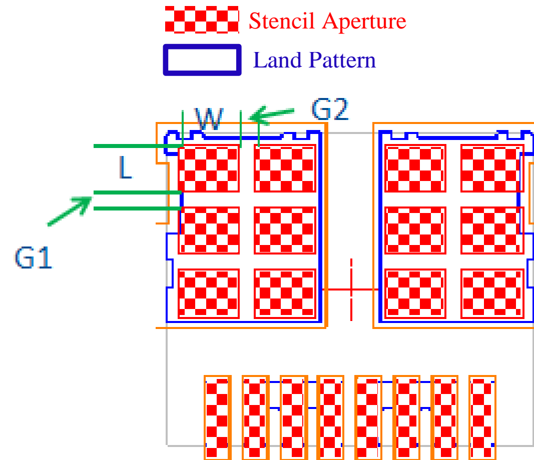



**Figure 10. Stencil Aperture Type 1: (Unit: mm)**

Stencil Structure Condition 2 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 | 1.36 | 1.79 | 0.60 | 0.60 | 0.12 | 3 | 2 | 42.8% | 34.12 | 5.38 | 6.48 |

- Type: No 2.
- 6 block rectangles
- Solder ratio: 42.8%
- Stencil thickness is 0.12mm

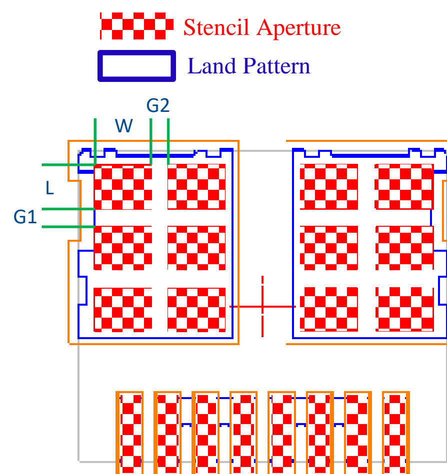



**Figure 11.Stencil Aperture Type 2: (Unit: mm)**

Stencil Structure Condition 3 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 1.23 | 1.64 | 0.70 | 0.70 | 0.12 | 3 | 2 | 35.4% | 34.12 | 5.38 | 6.48 |

- Type: No 3.
- 6 block rectangles
- Solder ratio: 35.4%
- Stencil thickness is 0.12mm

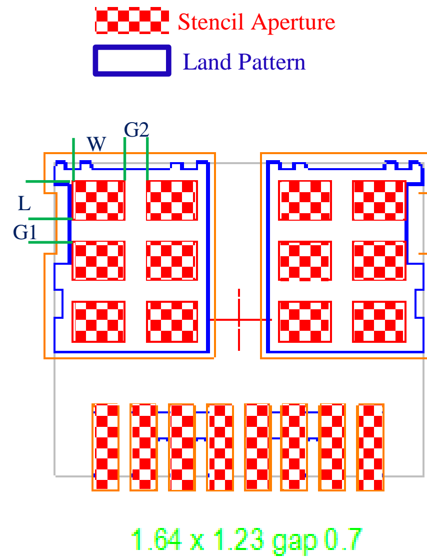



**Figure 12. Stencil Structure Type 3: (Unit: mm)**

Stencil Structure Condition 4 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 1.63 | 1.26 | 0.40 | 0.40 | 0.12 | 3 | 3 | 54.1% | 34.12 | 5.38 | 6.48 |

- Type: No 4.
- 9 block squares
- Solder ratio: 54.1%
- Stencil thickness is 0.12mm

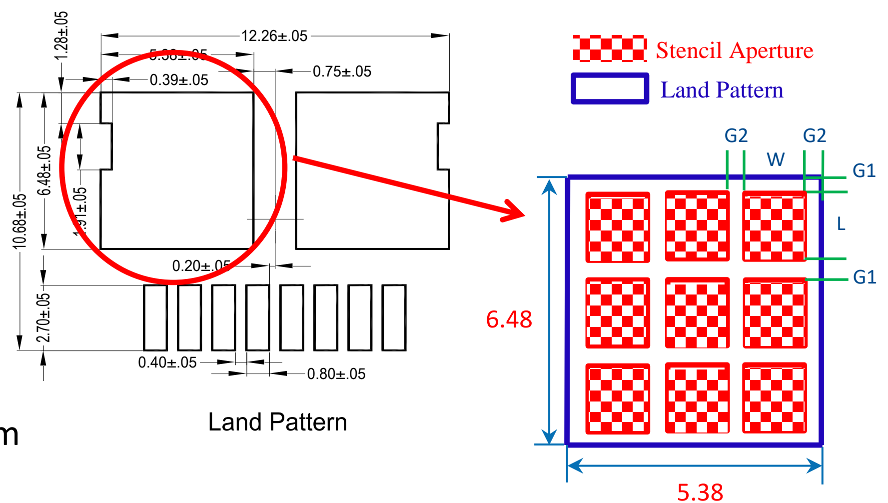
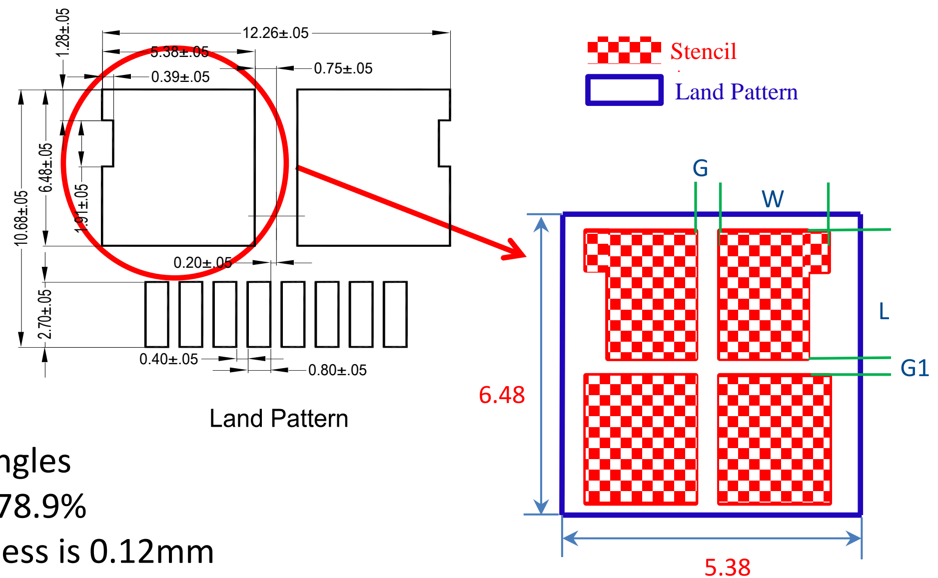



**Figure 13. Stencil Aperture Type 4: (Unit: mm)**

Stencil Structure Condition 5 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 | 2.84 | 2.37 | 0.50 | 0.50 | 0.12 | 2 | 2 | 78.9% | 34.12 | 5.38 | 6.48 |

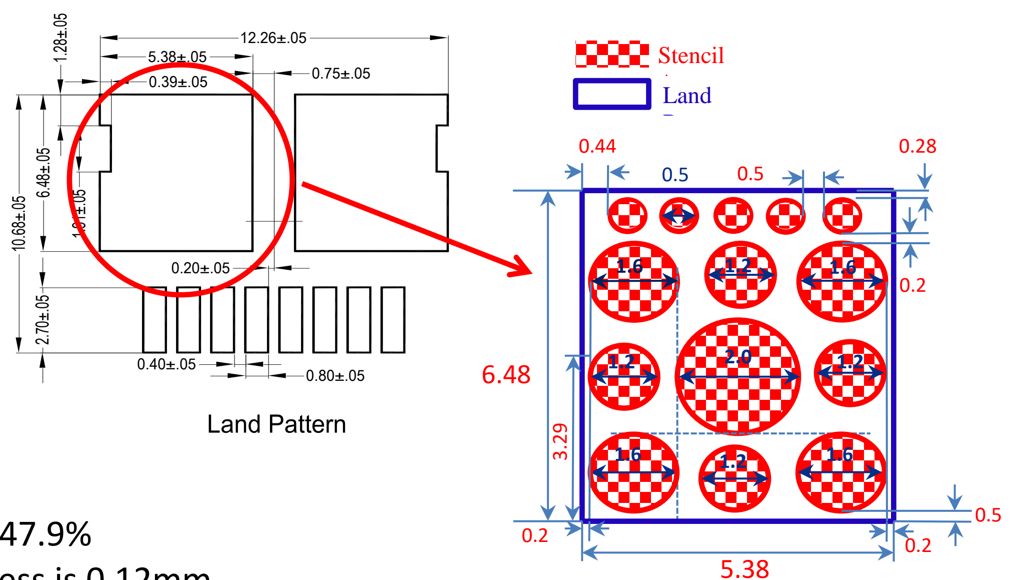



- Type: No 5.
- 4 block rectangles
- Solder ratio: 78.9%
- Stencil thickness is 0.12mm

**Figure 14.Stencil Aperture Type 5: (Unit: mm)**

Stencil Structure Condition 6 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|
| 6 | Circular -- 0.5mm x 5pcs / 1.2mm x 4pcs / 1.6mm x 4pcs / 2.0mm x 1pcs | | | | 0.12 | 47.9% | 34.12 | 5.38 | 6.48 |

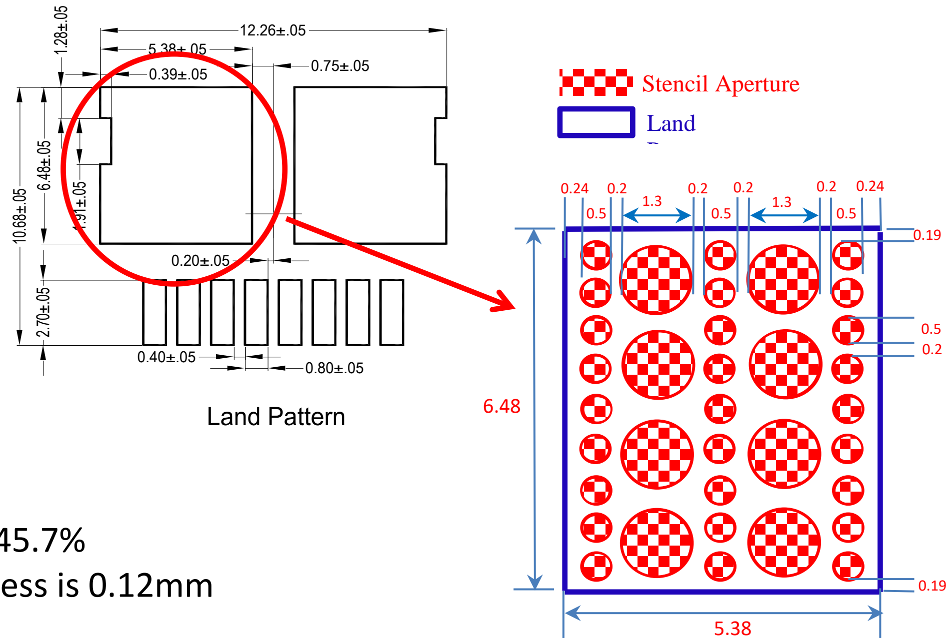



- Type: No 6.
- Circular
- Solder ratio : 47.9%
- Stencil thickness is 0.12mm

**Figure 15.Stencil Structure Condition 6: (Unit: mm)**

Stencil Structure Condition 7 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|
| 7 | Circular -- 0.5mm x 27pcs / 1.3mm x 8pcs | | | | 0.12 | 45.7% | 34.12 | 5.38 | 6.48 |

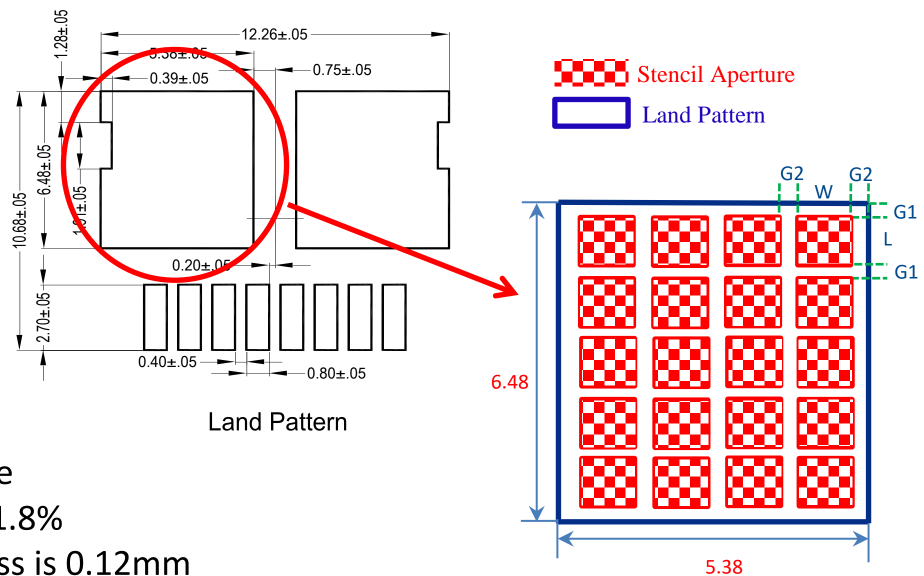



- Type: No 7.
- Circular
- Solder ratio: 45.7%
- Stencil thickness is 0.12mm

**Figure 16. Stencil Aperture Type 7: (Unit: mm)**

Stencil Structure Condition 8 : (Unit : mm)

| No | L | W | G1(L) | G2(W) | T(Thickness) | Opening Q'ty L | Opening Q'ty W | Solder Area ratio | Land pattern Area | Land pattern W | Land pattern L |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 | 0.93 | 0.97 | 0.30 | 0.30 | 0.12 | 5 | 4 | 51.8% | 34.12 | 5.38 | 6.48 |




- Type: No 8.
- 20 block square
- Solder ratio: 51.8%
- Stencil thickness is 0.12mm

**Figure 17.Stencil Structure Condition 8: (Unit: mm)**

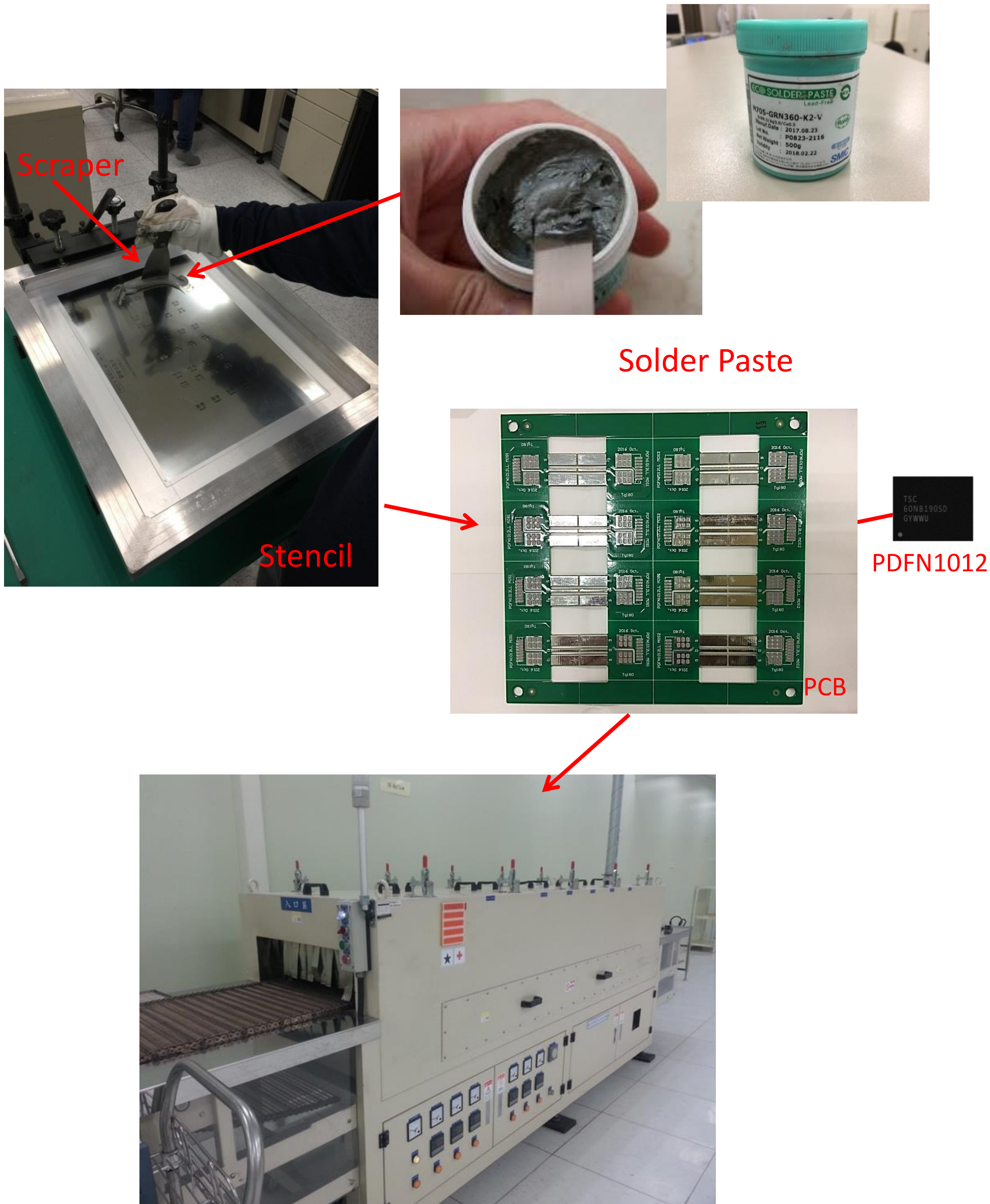
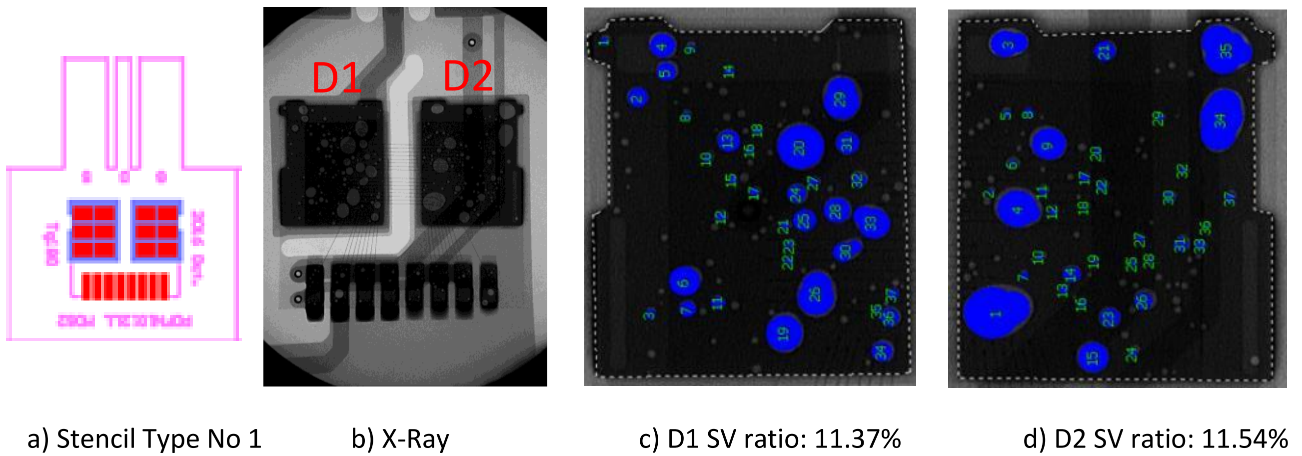



**Figure 18. Test PCB after screening solder paste and reflow process**

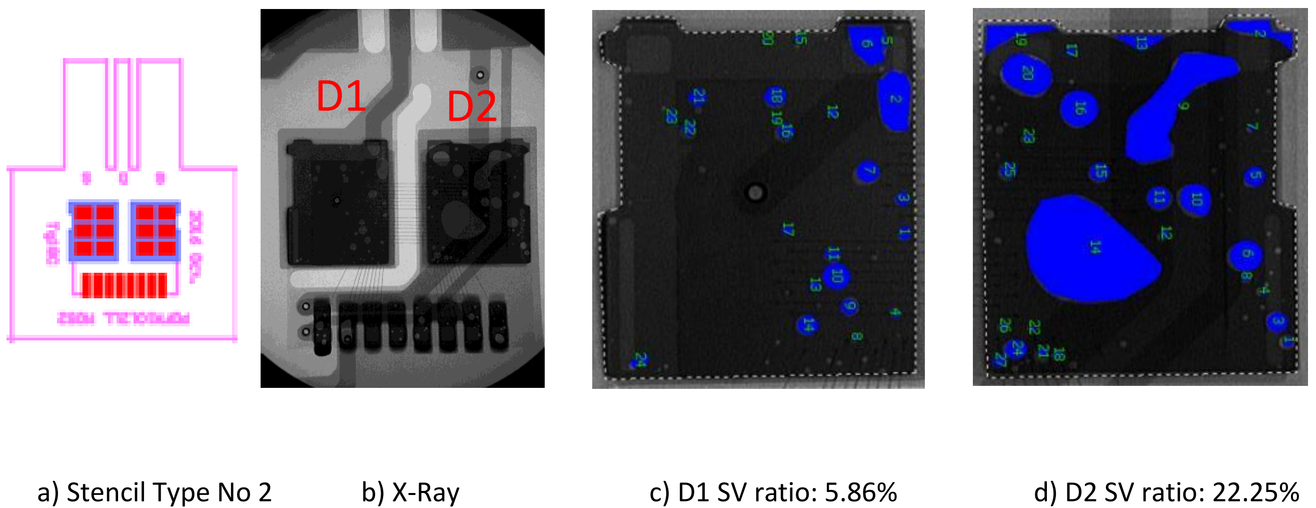
## Post Reflow X-Ray Inspection

Following reflow, X-Ray was used measure the resultant solder voids between PCB and component. Figures 19 – 26 show the voids measured and the calculated solder void ratio for each of the eight stencil aperture types used.



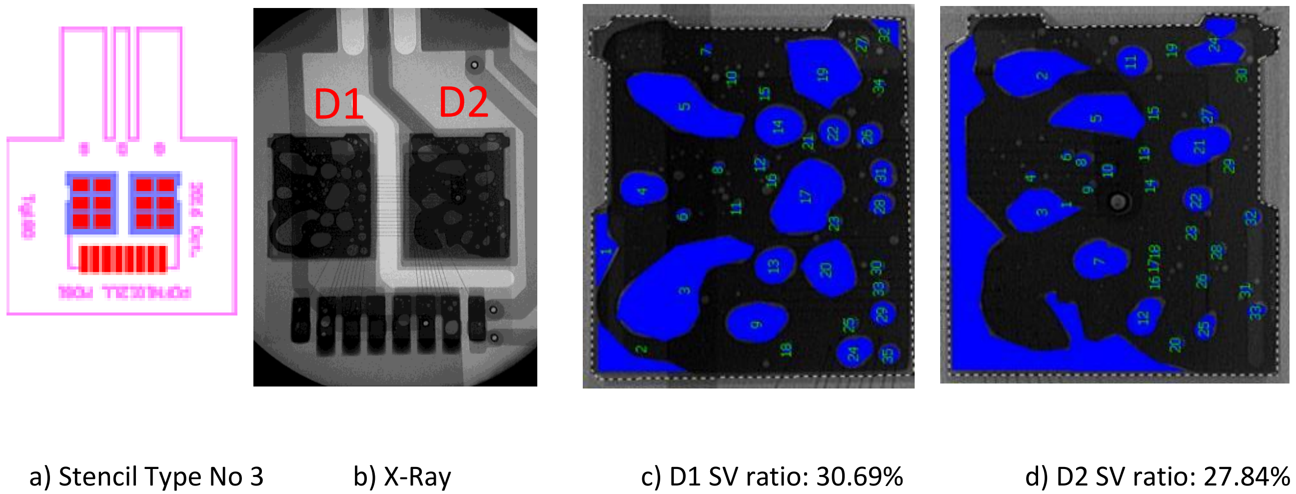

a) Stencil Type No 1 b) X-Ray c) D1 SV ratio: 11.37% d) D2 SV ratio: 11.54%

**Figure 19. Stencil Aperture Type 1 solder void (SV) ratio measurement (solder area ratio: 50.9%)**



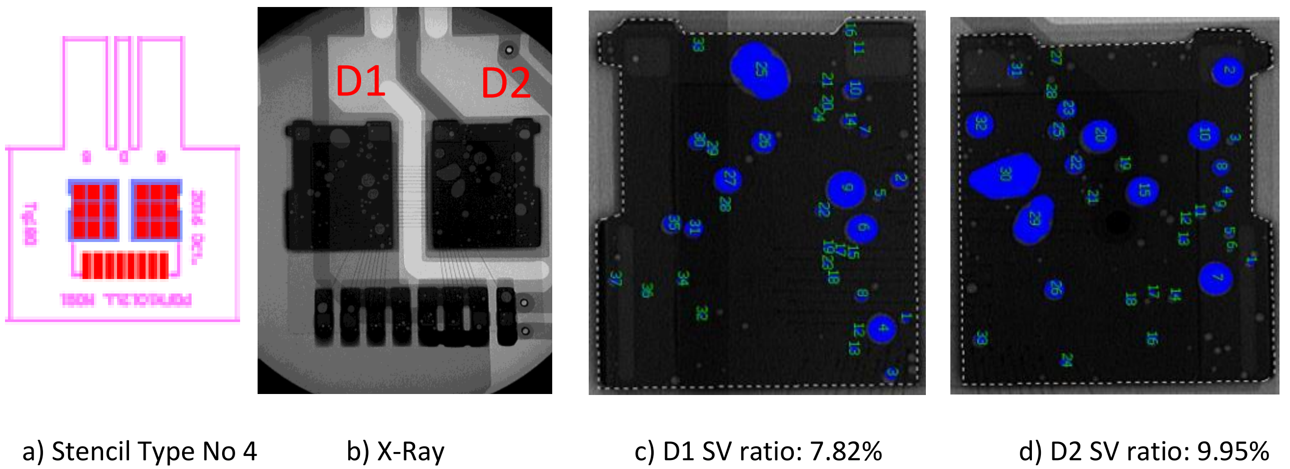

a) Stencil Type No 2 b) X-Ray c) D1 SV ratio: 5.86% d) D2 SV ratio: 22.25%

**Figure 20. Stencil Aperture Type 2 solder void (SV) ratio measurement (solder area ratio: 42.8%)**



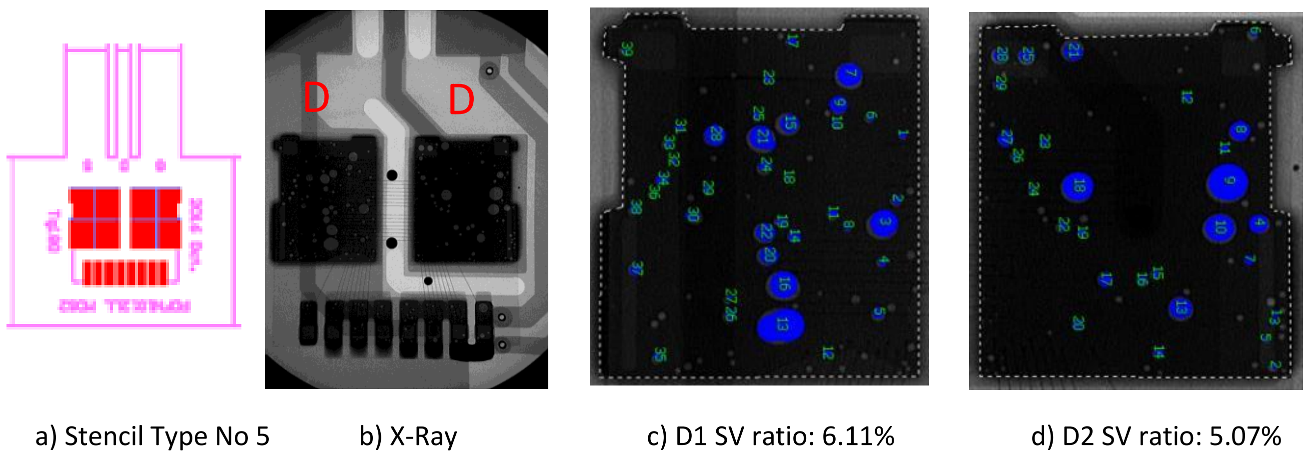

a) Stencil Type No 3 b) X-Ray c) D1 SV ratio: 30.69% d) D2 SV ratio: 27.84%

**Figure 21. Stencil Aperture Type 3 solder void (SV) ratio measurement (solder area ratio: 35.4%)**




a) Stencil Type No 4 b) X-Ray c) D1 SV ratio: 7.82% d) D2 SV ratio: 9.95%

**Figure 22. Stencil Aperture Type 4 solder void (SV) ratio measurement (solder area ratio: 54.1%)**




a) Stencil Type No 5 b) X-Ray c) D1 SV ratio: 6.11% d) D2 SV ratio: 5.07%

**Figure 23. Stencil Aperture Type 5 solder void (SV) ratio measurement (solder area ratio: 78.9%)**

a) Stencil Type No 6 b) X-Ray c) D1 SV ratio: 12.88% d) D2 SV ratio: 21.33%

**Figure 24. Stencil Aperture Type 6 solder void (SV) ratio measurement (solder area ratio: 47.9%)**

a) Stencil Type No 7 b) X-Ray c) D1 SV ratio: 18.58% d) D2 SV ratio: 7.22%

**Figure 25. Stencil Aperture Type 7 solder void (SV) ratio measurement (solder area ratio: 45.7%)**

a) Stencil Type No 8 b) X-Ray c) D1 SV ratio: 11.05% d) D2 SV ratio: 7.98%

**Figure 26. Stencil Aperture Type 8 solder void (SV) ratio measurement (solder area ratio: 51.8%)**

## Solder void density measurement summary

From a thermal performance, and solder joint reliability perspective smaller void area with respect to the PCB land is very important.

IPC-A-610 industry standard requires the total area ratio to be less 25%, and most companies design their PCB and manufacturing processes to maintain less than a 15% ~ 25% solder void ratio. For this study, there were four test PCBs measured, each PCB included the eight stencil aperture designs and each stencil aperture design had two equivalent openings associated with D1 and D2. This results in a total of 64 solder void ratio measurements. Table 2 summarizes the results of these 64 solder void ratio measurements.

Analysis of the results indicates aperture type 4 and 5 are the best aperture designs from those tested. Both aperture designs resulted in an average of <10% solder void ratio which will maintain the thermal and reliability performance of the component in application very well.

**Table 2. Measured solder void ratio summary of the eight stencil aperture types.**

| Solder void ratio | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Stencil opening ratio | | No 1 | No 2 | No 3 | No 4 | No 5 | No 6 | No 7 | No 8 |
| | | 50.90% | 42.80% | 35.40% | 54.10% | 78.90% | 47.90% | 45.70% | 51.80% |
| 1 | D1 | 11.37% | 22.25% | 30.69% | 9.95% | 5.07% | 12.88% | 7.22% | 11.05% |
| | D2 | 11.54% | 5.86% | 27.84% | 7.82% | 6.11% | 21.33% | 18.58% | 7.98% |
| 2 | D1 | 9.88% | 28.59% | 29.77% | 6.23% | 8.83% | 9.79% | 11.17% | 10.95% |
| | D2 | 20.67% | 19.80% | 32.00% | 8.24% | 6.45% | 7.01% | 21.24% | 14.30% |
| 3 | D1 | 7.39% | 14.08% | 28.72% | 5.10% | 7.34% | 16.04% | 8.80% | 9.93% |
| | D2 | 13.62% | 11.47% | 38.70% | 7.21% | 11.47% | 10.05% | 15.79% | 12.28% |
| 4 | D1 | 9.54% | 19.35% | 23.20% | 5.24% | 6.38% | 9.11% | 14.57% | 15.02% |
| | D2 | 11.36% | 14.95% | 29.34% | 7.11% | 12.44% | 25.61% | 7.89% | 25.08% |
| Max | | 20.67% | 28.59% | 38.70% | 9.95% | 12.44% | 25.61% | 21.24% | 25.08% |
| Min | | 7.39% | 5.86% | 23.20% | 5.10% | 5.07% | 7.01% | 7.22% | 7.98% |
| AVG | | 11.92% | 17.04% | 30.03% | 7.11% | 8.01% | 13.98% | 13.16% | 13.32% |

## Summary and Conclusions

Large area, thin, leadless packages face design implementation challenges to ensure the integrity and long-term reliability of a power semiconductor component as it is soldered on to the application PCB. Robust signal and power pin solder volume, solder fillet, and low solder void density following reflow are necessary to maintain the high power density performance offered by these packages.

This application note highlights the Taiwan Semiconductor PDFN1012 package features that ensure robust and reliable solderability. This study also provides solder stencil aperture design attributes that significantly minimize solder voids under the power tabs of the PDFN1012 package to provide a high level of efficient thermal performance and long term solder joint reliability.

The PDFN1012 package includes a “Natural Fillet” design that is shown to allow higher solder volume and better fillet definition at the package pins when compared to a similar package without the “natural Fillet structure.

Furthermore, the study indicates that a rectangular (square) solder island array stencil aperture design that provides between 54% and 79% solder coverage on the PCB power tab land results in the lowest void density.

**References**

1. IPC7525 - IPC Standard Stencil Design Guidelines
2. IPC-A-610 - IPC Standard Acceptability of Electronic
3. TSC PDFN1012 with Natural Fillet Design - Author: Sen Mao
4. TSM60NB190SDLL Datasheet - 600V PDFN1012 Dual N-Channel Common Source Power MOSFET

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