TAIWAN SEMICONDUCTOR

AN-1001

Understanding Power MOSFET Parameters

Content

MOSFET datasheet parameters introduction

Introduction

When choosing a MOSFET, parameters that are focused on by most engineers intuitively are V_{DS}, $R_{DS(on)}$, I_D. However, in power systems, it is significant to pick up a suitable MOSFET based on different applications. In this application note, Taiwan Semiconductor (TSC) introduces the definition of every single parameter of a MOSFET, and from chapter 3, TSC also explains how each parameter is realized, hoping this would help designers on the power projects.

1. Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)					
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**	**Notes**
Drain-Source Voltage		V_{DS}	30	V	**1.1**
Gate-Source Voltage		V_{GS}	±20	V	**1.2**
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	39	A	**1.3**
	T_A = 25°C		11		
Pulsed Drain Current		I_{DM}	156	A	**1.4**
Single Pulse Avalanche Current (Note 2)		I_{AS}	15.6	A	**1.5**
Single Pulse Avalanche Energy (Note 2)		E_{AS}	36.5	mJ	**1.6**
Total Power Dissipation	T_C = 25°C	P_D	33	W	**1.7**
	T_C = 125°C		6.6		
Total Power Dissipation	T_A = 25°C	P_D	2.6	W	
	T_A = 125°C		0.5		
Operating Junction and Storage Temperature range		T_J, T_{STG}	- 55 to +150	°C	**1.8**

1.1 Drain-Source Voltage (V_{DS})

V_{DS} represents MOSFET absolute maximum voltage between Drain and Source. In operations, voltage stress of Drain-Source should not exceed maximum rated value.

1.2 Gate-Source Voltage (V_{GS})

V_{GS} represents operating driver voltage between Gate and Source. In operations, voltage stress of Gate-Source should not exceed maximum rated value.

1.3 Continuous Drain Current (I_D)

I_D represents MOSFET's continuous conduction current and could be calculated by below equation.

$$I_D = \sqrt{\frac{T_J - T_C}{R_{\theta JC} \times R_{DS(ON)} \times K}}$$

T_J = Junction Temperature

T_C = Case Temperature

$R_{DS(ON)}$ = Drain-Source On-State Resistance

$R_{\theta JC}$ = Junction to Case Thermal Resistance

K = On-Resistance vs. Junction Temperature

1.4 Pulsed Drain Current (I_{DM})

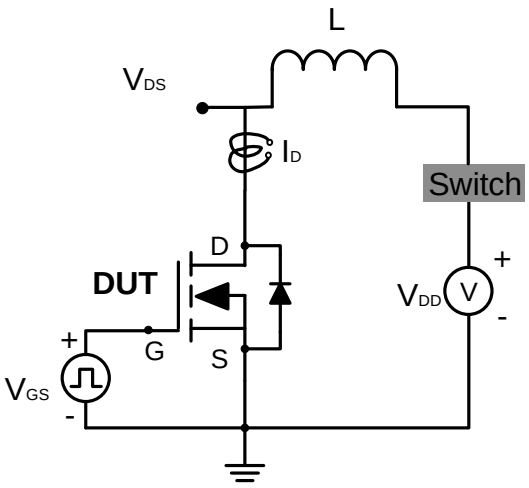
I_{DM} represents maximum limit current in MOSFET SOA (Safe Operating Area). A MOSFET could be well operated within SOA to make sure the stability and safety of a power system.

1.5 Single Pulse Avalanche Current (I_{AS})

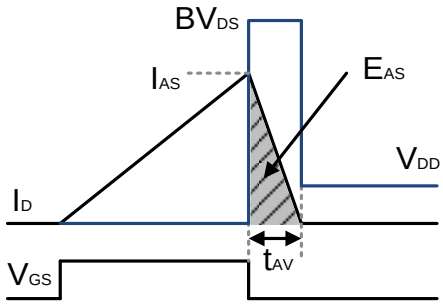
When power MOSFET enters the avalanche mode, the current transformed into the form of voltage across Drain and Source of a MOSFET is called avalanche current (I_{AS}).

1.6 Single Pulse Avalanche Energy (E_{AS})

UIL (unclamped inductive load) or UIS (unclamped inductive switching) tests are important to check the degree of robustness of a power MOSFET. E_{AS} represents allowed maximum energy in either one pulse that is over rated V_{DS}. When the operating voltage exceeds the specified V_{DS} at off state of a MOSFET, it will enter the avalanche mode and cause high power dissipation. The parameter is often taken into consideration when inductive load or transient loading is operated.



UIS Test Circuit



$$E_{AS} = \frac{1}{2} \times L \times I_{AS}^{\ 2} \times \left(\frac{BV_{DS}}{BV_{DS} - V_{DD}}\right)$$

The UIS test circuit: When applying a V_{GS} signal to a DUT and the DUT is turned on, the current will start to charge Inductor (L), phenomenon of the I_D current rising rate behaves linearly as above picture. When the required I_D is reached to I_{AS}, the DUT is then turned off, causing the Inductor to dissipate all of its stored energy and enforcing the DUT to reach its breakdown voltage rating. The DUT will remain in breakdown (BV_{DS}) until all of the energy is dissipated. The blue area is E_{AS} (Energy Avalanche Single).

1.7 Total Power Dissipation (P_D)

P_D represents the capability of maximum power dissipation that a MOSFET can handle. Moreover, capability of power dissipation varies by different temperature conditions.

When case temperature (T_C) is considered, equation would be:

$$P_D = \frac{T_J - T_C}{R_{\theta JC}}$$

As for ambient temperature (T_A), equation turns into:

$$P_D = \frac{T_J - T_A}{R_{\theta JA}}$$

T_J = Junction Temperature
T_C = Case Temperature
$R_{\theta JC}$ = Junction to Case Thermal Resistance
$R_{\theta JA}$ = Junction to Ambient Thermal Resistance

1.8 Operating Junction and Storage Temperature Range (T_J, T_{STG})

T_J represents maximum operating temperature of a MOSFET. A MOSFET should be avoided to be operated over the rated temperature limit.

T_{STG} represents the range of temperature for storage or transportation of a MOSFET. It must be storage in specified temperature values.

2. Thermal Performance

THERMAL PERFORMANCE				
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**	**Notes**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	3.8	°C/W	**2.1**
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	48	°C/W	**2.2**

2.1 Junction To Case Thermal Resistance ($R_{\Theta JC}$)

$R_{\Theta JC}$ is the sum of the junction to case thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.

2.2 Junction To Ambient Thermal Resistance ($R_{\Theta JA}$)

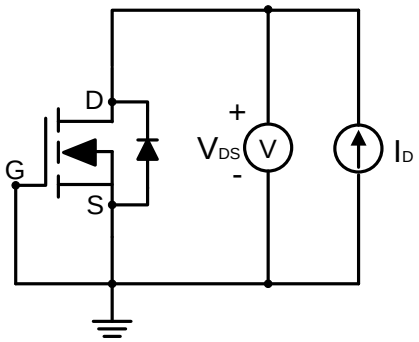
$R_{\Theta JA}$ is the sum of the junction to case and case to ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

3. Electrical Specifications

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**Notes**
Static							
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	30	--	--	V	**3.1**
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	1.2	1.9	2.5	V	**3.2**
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA	**3.3**
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 30V	I_{DSS}	--	--	1	μA	**3.4**
	V_{GS} = 0V, V_{DS} = 30V T_J = 125°C		--	--	100		
Drain-Source On-State Resistance **(Note 3)**	V_{GS} = 10V, I_D = 11A	$R_{DS(on)}$	--	8.3	11.7	mΩ	**3.5**
	V_{GS} = 4.5V, I_D = 11A		--	11.9	14.9		
Forward Transconductance **(Note 3)**	V_{DS} = 5V, I_D = 11A	g_{fs}	--	35	--	S	**3.6**

3.1 Drain-Source Breakdown Voltage (BV_{DSS})

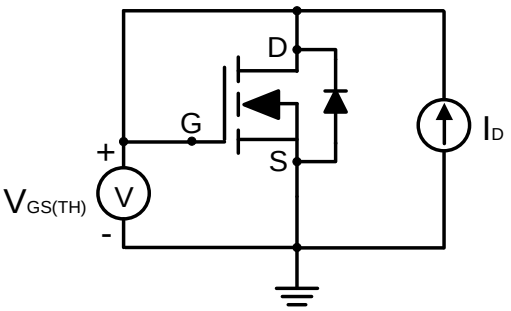
To measure breakdown voltage of a MOSFET, at first, short Gate pin and Source pin, and then, supply the I_D=250μA, and monitor the reading of V_{DS}.



BV_{DSS} is determined when I_D reaches 250μA. Gate pin is shorted to Source pin.

3.2 Gate Threshold Voltage ($V_{GS(TH)}$)

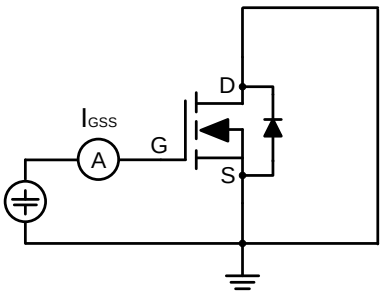
To measure gate threshold voltage of a MOSFET, at first, short Gate pin and Drain pin, and then, with a given I_D=250μA, and monitor the voltage difference between Gate-Source. One significant characteristics of $V_{GS(TH)}$ is its negative temperature coefficient. If power system has to be operated at a certain minus degree, to avoid unpredicted being turned on, $V_{GS(TH)}$ needs to be taken into consideration.



$V_{GS(TH)}$ is determined when I_D reaches 250μA. Gate pin is shorted to Drain pin.

3.3 Gate-Source Leakage Current (I_{GSS})

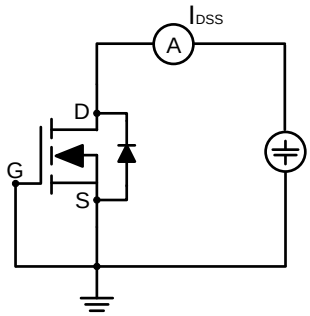
To measure Gate-Source leakage current of a MOSFET, at first, short Drain pin and Source pin, and then, apply maximum allowable voltage on Gate-Source and monitor the leakage current of Gate-Source. I_{GSS} is dependent on the structure and design of the gate oxide.



I_{GSS} is determined when maximum V_{GS} voltage is applied. Drain pin is shorted to source pin

3.4 Drain-Source Leakage Current (I_{DSS})

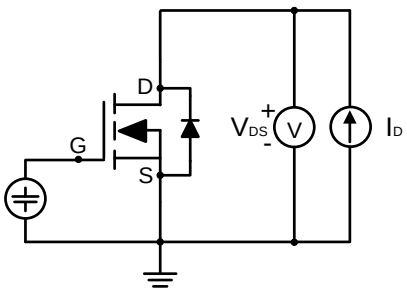
To measure Drain-Source leakage current of a MOSFET, at first, short Gate pin and Source pin, and then, apply maximum allowable voltage on Drain-Source and monitor the leakage current of Drain-Source.



I_{DSS} is determined when maximum V_{DS} voltage is applied. Gate pin is shorted to Source pin

3.5 Drain-Source On-State Resistance ($R_{DS(on)}$)

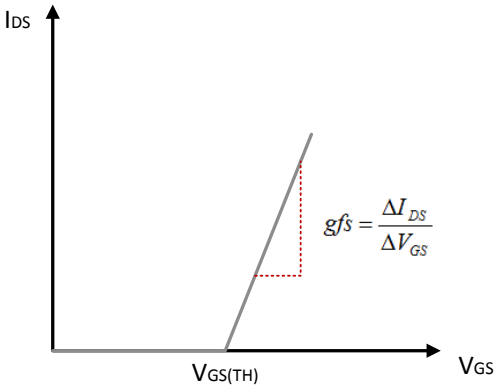
To measure Drain-Source on resistance, $R_{DS(on)}$, at first, apply a voltage across Gate-Source, which is specified to be higher than $V_{GS(TH)}$. With a given current source, I_D, measure the voltage drop across Drain-Source, V_{DS}. And after that, through the equation, $R_{DS(on)} = V_{DS} / I_D$, $R_{DS(on)}$ is observed. In TSC MOSFET datasheet, two additional figures are introduced as well. One is $R_{DS(on)}$ vs V_{GS} graph since $R_{DS(on)}$ varies by different amplitude of V_{GS}. The other one is $R_{DS(on)}$ vs T_J. Characteristics of $R_{DS(on)}$ is positive temperature coefficient. It is important to consider the surrounding temperature of selecting a MOSFET in a power system.



Apply specified V_{GS}, and given I_D, measured V_{DS} of a MOSFET, then $R_{DS(on)}$ is obtained

3.6 Forward Transconductance (g_{fs})

Forward transconductance, g_{fs}, represents the signal gain (drain current divided by gate voltage) of a MOSFET. Higher g_{fs} indicates the high current (I_{DS}) handling capability can be gained from the low gate voltage (V_{GS}). It is also expressed as below equation.



4. Dynamic

Dynamic (Note 4)							
Total Gate Charge	V_{GS} = 10V, V_{DS} = 15V, I_D = 11A	Q_g	--	9.2	--	nC	**4.1**
Total Gate Charge	V_{GS} = 4.5V, V_{DS} = 15V, I_D = 11A	Q_g	--	4.5	--	nC	**4.1**
Gate-Source Charge		Q_{gs}	--	1.9	--	nC	**4.1**
Gate-Drain Charge		Q_{gd}	--	1.7	--	nC	**4.1**
Input Capacitance	V_{GS} = 0V, V_{DS} = 15V f = 1.0MHz	C_{iss}	--	562	--	pF	**4.2**
Output Capacitance		C_{oss}	--	144	--	pF	**4.2**
Reverse Transfer Capacitance		C_{rss}	--	50	--	pF	**4.2**
Gate Resistance	f = 1.0MHz, open drain	R_g	0.5	1.7	3.4	Ω	**4.3**

4.1 Total Gate Charge (Q_g)

Gate charge plays prominently in high frequency switching applications. Total gate charge Q_g include Q_{gs} and Q_{gd}. Q_{gs} represents the accumulation of Gate-Source capacitance while Q_{gd} is the accumulation of Gate-Drain capacitance, also called miller capacitor. In high frequency operations, Q_g should be selected as small as possible. Another tip of Gate charge for picking up a MOSFET in H-bridge power system design is that ratio of Q_{gd}/Q_{gs} be lower than 1 to prevent the circuit from shoot through.

4.2 Capacitances (C_{iss}, C_{oss}, C_{rss})

C_{iss}, C_{oss}, and C_{rss}, like gate charge, also influence on switching performance. In TSC MOSFET Datasheet, either one would be tested at various Drain-Source voltages and under 1MHz frequency conditions. Relationships of MOSFET capacitances are listed below.

$$C_{iss} = C_{gs} + C_{gd}$$
$$C_{oss} = C_{ds} + C_{gd}$$
$$C_{rss} = C_{gd}.$$

4.3 Gate Resistance (R_g)

R_g is designed and implemented inside gate area. And with the help of MOSFET embedded Rg, the external gate drive circuit could be simplified.

5. Switching time

Switching (Note 4)							
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 15V, I_D = 7A, R_G = 10Ω,	$t_{d(on)}$	--	8.4	--	ns	**5.1**
Turn-On Rise Time		t_r	--	4.3	--		
Turn-Off Delay Time		$t_{d(off)}$	--	22.4	--		
Turn-Off Fall Time		t_f	--	3.1	--		

5.1 Switching Time ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f)

Switching time includes $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f four main parameters and also represent important impact on switching loss of MOSFET. Each one is described as below.

$t_{d(on)}$ – Turn-on Delay Time

The turn-on delay time is defined as the time interval measured between 10% of V_{GS} rising from zero and 90% of V_{DS} falling from rated voltage.

t_r – Rise Time

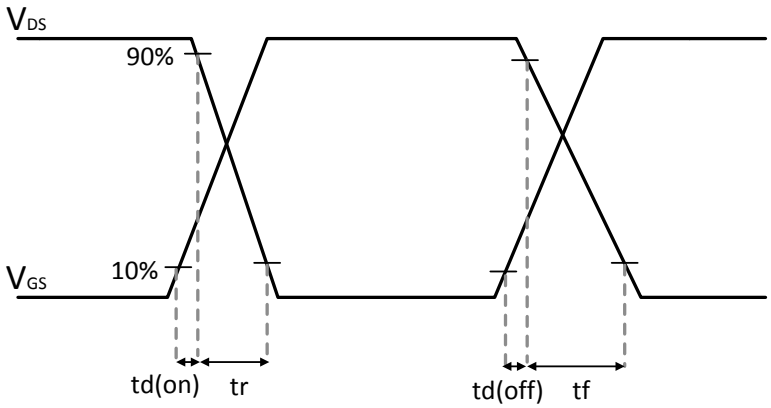
t_r represents the time interval between V_{DS} falling from 90% to 10% of rated voltage. I_D starts to rise and is considered to be the major turn-on losses during this period.

$t_{d(off)}$ – Turn-off Delay Time

The turn-off delay time is defined as the time interval measured between 10% of V_{DS} rising from zero and 90% of V_{GS} falling from rated voltage.

t_f – Fall Time -

t_f represents the time interval between V_{DS} rising from 10% to 90% of rated voltage. I_D starts to fall and is considered to be the major turn-off losses during this period.

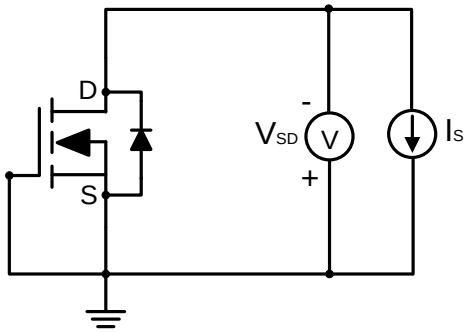


6. Source-Drain Diode Characteristics

Source-Drain Diode							
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 11A	V_{SD}	--	--	1.2	V	**6.1**
Reverse Recovery Time	I_S = 11A , dI/dt = 100A/μs	t_{rr}	--	14.7	--	ns	**6.2**
Reverse Recovery Charge		Q_{rr}	--	7.3	--	nC	

6.1 Forward Voltage (V_{SD})

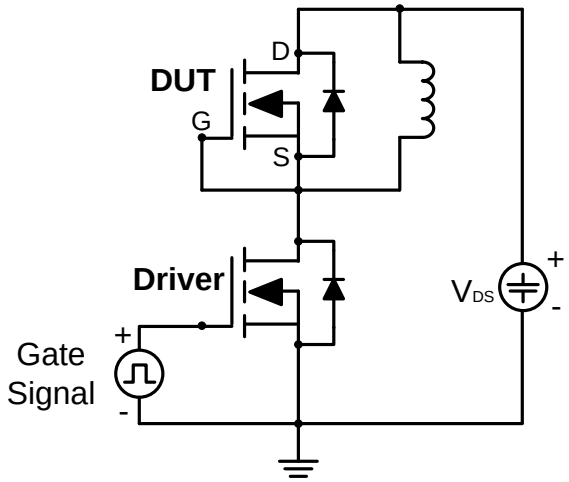
To measure Source-Drain voltage, VSD, at first, short Gate pin and Source pin. Apply a specified reverse current, I_S, and V_{SD} is measured.

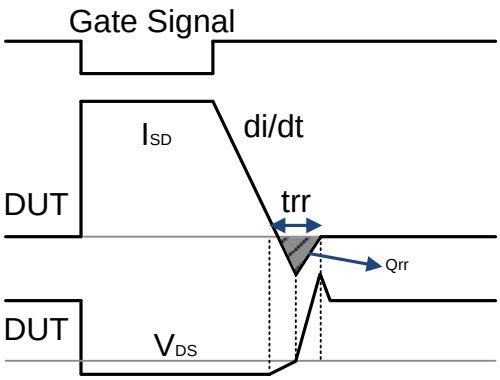


The V_{SD} is measured by applying I_S current. Gate pin is shorted to Source pin.

6.2 Body Diode Reverse Recovery (t_{rr} , Q_{rr})

To measure reverse recovery time, t_{rr} and reverse recovery charge, Q_{rr}, at first, short Gate pin and Source pin of DUT MOSFET. Moreover, a gate drive circuit, a given voltage source, V_{dd}, and an inductor are required to form a diode recovery test circuit. When MOSFET of gate drive circuit is turned on, L is charged; when it is turned off, energy of inductor will be discharged through intrinsic body diode of DUT MOSFET. When MOSFET of gate drive circuit is turned on again, the body diode of DUT will be reversed biased and reverse recovery starts to behave. t_{rr} and Q_{rr} are measured.



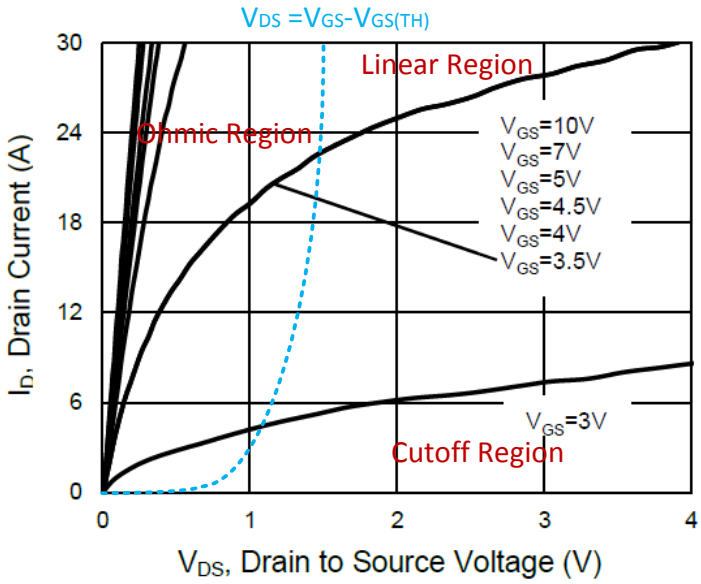


t_{rr} and Q_{rr} are measured through above test circuit. Short Gate pin and Source pin of DUT MOSFET In applications, when I_{SD} reaches back to zero, the voltage spike happens on Drain-Source due to inductor energy released to C_{oss} of MOSFET. Higher Q_{rr} would cause severe voltage spike and vice versa.

7. Characteristics Curves

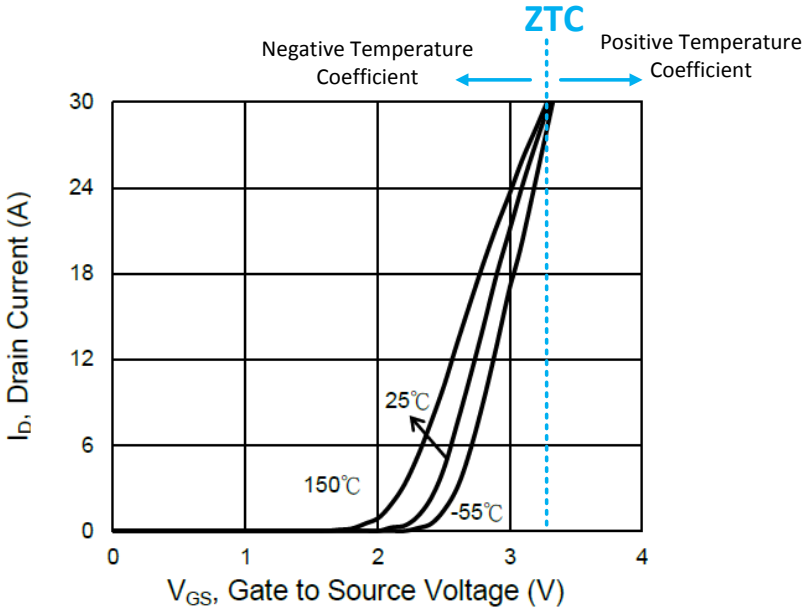
(T_A = 25°C unless otherwise noted)

Output Characteristics



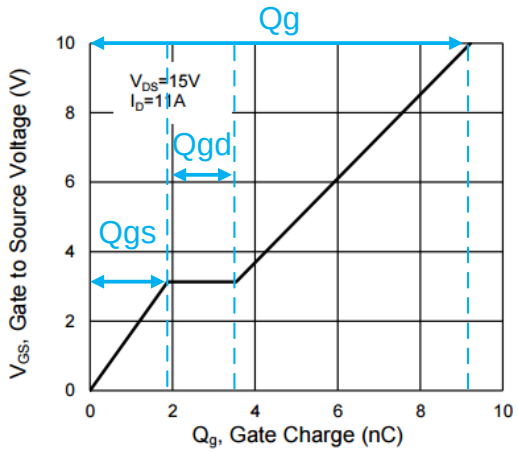
In output characteristics, three major regions are introduced, Ohmic region, Linear region, and Cut off region. The figure also shows curve defined by I_D vs V_{DS} at various gate to source voltage conditions. When MOSFET is turned on with $V_{GS} < V_{GS(TH)}$, it is operated in cut off region , when $V_{DS} > V_{GS}-V_{GS(TH)}$, it is operated at linear region. Finally, when $V_{DS} < V_{GS}-V_{GS(TH)}$, it is operated in Ohmic region. The blue dash line is defined by $V_{DS} = V_{GS} – V_{GS(TH)}$.

Transfer Characteristics

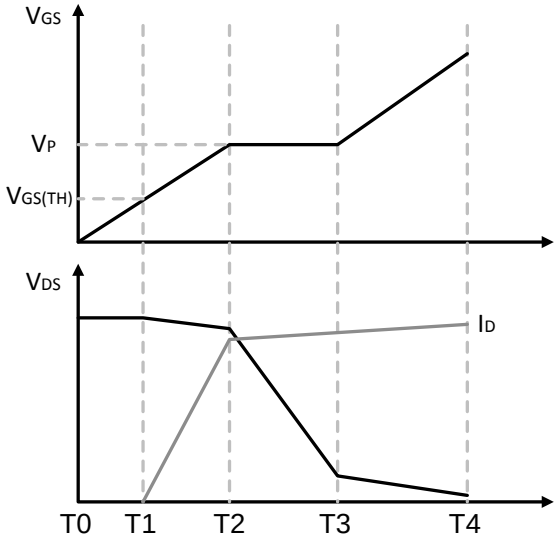


The transfer characteristics curve represents both V_{GS} and I_D relationship. From above, there is a ZTC point (Zero Temperature Coefficient). If V_{GS} is under ZTC point, V_{GS} becomes a negative temperature coefficient and vice versa.

Gate-Source Voltage vs. Gate Charge



Gate charge include 3 specified values, Qgs, Qgd ,and Qg. Qgs denotes Gate to Source charge. Qgd denotes Gate to Drain charge, which is also called the miller effect charge. Qg denotes the total gate charge.



Operations of Gate Charge are presented as below from above diagram.

1. T0 ~ T1

   When V_{GS} rises and reaches to $V_{GS(TH)}$, C_{GS} is the capacitor to be charged. At the time, both I_D and V_{DS} present unchanged.

2. T1 ~ T2

   At this time interval, MOSFET is working in linear region. V_{GS} continues stepping up to the plateau voltage, V_P. C_{GS} is completely charged and I_D is raised up to full load current.

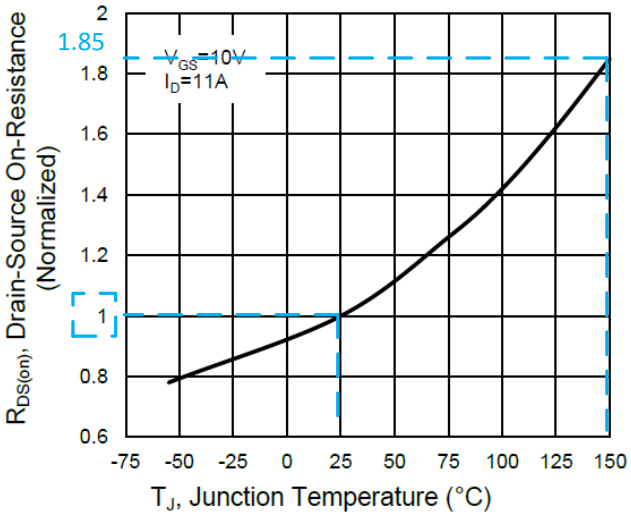
3. T2 ~ T3

   At this time interval, MOSFET is still working in linear region. And, V_{DS} voltage starts to decrease and finally drops to zero. So the C_{GD} * (dV_{DS}/dt) becomes big and thus, creates current flowing through C_{GD}, which blocks V_{GS} keeps rising and maintains constant. During this time, $R_{DS(on)}$ changes from high impedance to low impedance, entering Ohmic region.

4. T3 ~ T4

   In this timing, V_{GS} is raised up to rated value and MOSFET is operated in Ohmic region.

On-Resistance vs. Junction Temperature

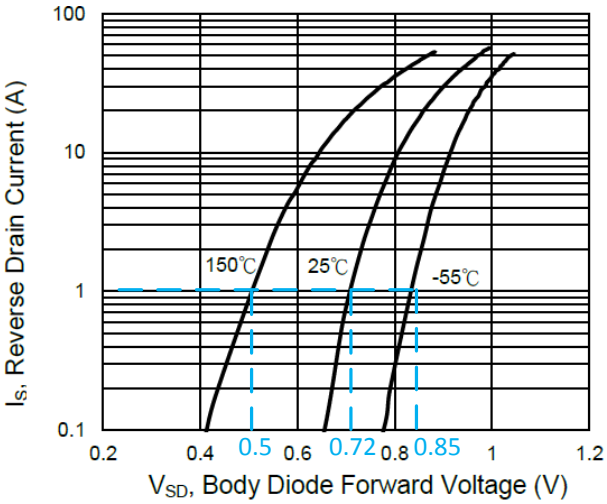


From the curve of $R_{DS(on)}$ vs. T_J, it's seen the normalized $R_{DS(on)}$ is 1 at T_J=25°C, and 1.85 at T_J=150°C. This indicates if the RDS(on) is 12mohm at T_J=25°C, it is expected to be 22.2 mohm at T_J=150°C.

$$\underline{K} = (K_{-150^\circ C} / K_{-25^\circ C}) = 1.85 / 1 \Rightarrow 1.85$$

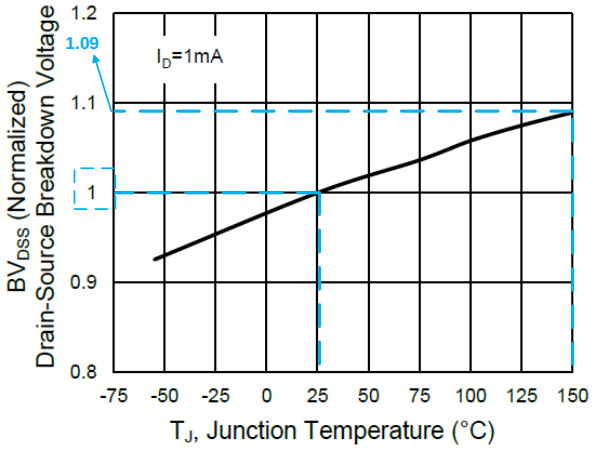
$\because R_{DS(on)}$ = 12mohm $\quad \therefore \underline{R_{DS(on)-150^\circ C}} = (R_{DS(0n)-25^\circ C} \times K) = 12\text{mohm} * 1.85 \Rightarrow 22.2\text{ mohm}$

Source-Drain Diode Forward Current vs. Voltage



From above curve, it is easily seen V_{SD} has negative temperature coefficient. So, it is expected to obtain lower V_{SD} voltage at higher temperature. From curve remarked, V_{SD} is 0.5V at T_J=150°C; V_{SD} is 0.72V at T_J=25°C; V_{SD} is 0.85V at T_J=-55°C.

BV_{DSS} vs. Junction Temperature

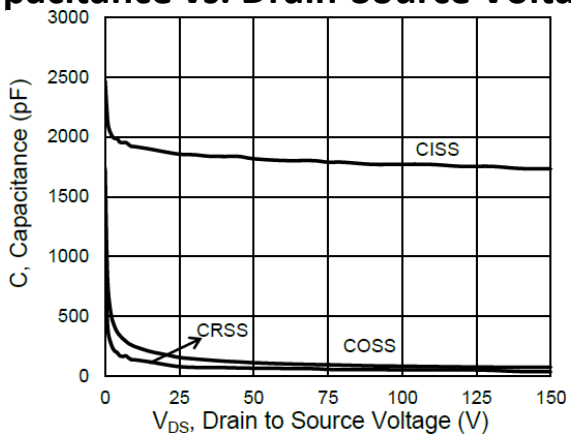


Above curve is BV_{DSS} vs. T_J. BV_{DSS} is positive temperature coefficient. Based on above curve, It is seen the normalized BV_{DSS} is 1 at T_J=25°C, and 1.09 at T_J=150°C. That is, if the BV_{DSS} is 30V at T_J=25°C, it is expected BV_{DSS} is 32.7V at T_J=150°C.

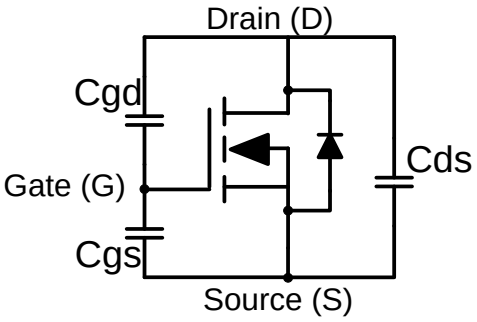
$$\underline{K} = (K_{-150°C} / K_{-25°C}) = 1.09 / 1 \Rightarrow 1.09$$

$\because$ BV_{DSS} = 30V $\quad\quad$ $\therefore \underline{BV_{DSS-150°C}} = (BV_{DSS-25°C} \times K) = 30V * 1.09 \Rightarrow 32.7V$

Capacitance vs. Drain-Source Voltage

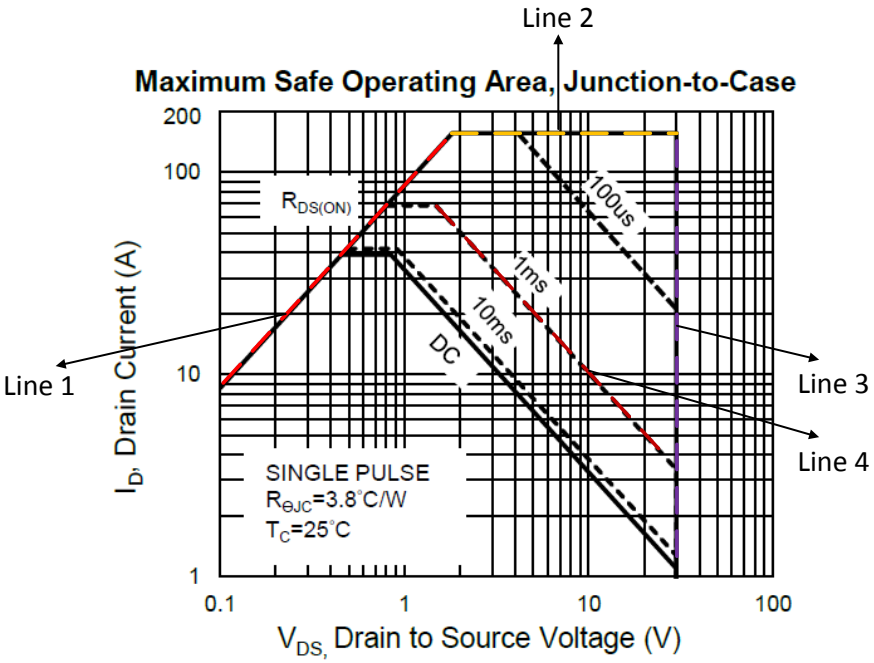


MOSFET have three types capacitances, Ciss, Coss and Crss. Regarding to the relationship of these capacitances, V_{DS} voltage and frequency, it is introduced from above curve with a fixed frequency to observe to variations of C_{iss}, C_{oss}, and C_{rss}. These three capacitances will affect the switching loss of power system. Below shows defined three types capacitances.



MOSFET Equivalent Circuit

SOA



SOA is defined the maximum value of V_{DS}, I_D and time envelope of operation which guarantees safe operation when MOSFET works is actively biased. Four lines are used to determine the maximum operating limits.

Line 1

$R_{DS(on)}$ limits. For example, take TSC 30V MOSFET as example, whose maximum $R_{DS(on)}$ is 11.7 mohm. According to the ohm's law, when V_{DS} is 1.0V and $R_{DS(on)}$ is 11.7 mohm. I_D = 1.0V / 11.7mohm = 85.47A.

Line 2

The I_{DM} is defined by Pulsed Drain Current of datasheet. It is based on the I_D@T_C 25°C value and generally speaking, I_{DM} = 4 × I_D(@T_C 25°C)

$$I_D = \sqrt{\frac{T_J - T_C}{R_{\theta JC} \times K \times R_{ds(on)}}} \quad @25°C$$

Line 3

This line is limited by the breakdown voltage.

Line 4

This line is limited by the a lot of parameters, including T_J, T_C, P_D, $R_{\theta JC}$, $Z_{\theta JC}$, and K factor ($R_{DS(on)}$ vs. T_J). The normalized effective transient thermal impedance ($Z_{\theta JC}$) depends on different square wave pulse duration(t) then got the both P_D and I_D from below equation.

For example, take TSC 30V MOSFET as example:

V_{DS} = 30V, $R_{\theta JC}$ is 3.8°C/W, $Z_{\theta JC}$ is $0.31@1\text{mS}$

$$P_D = \frac{T_J - T_C}{R_{\theta JC} \times Z_{\theta JC}} \qquad I_D = \frac{P_D}{V_{DS}}$$

P_D = (150°C - 25°C)/(3.8°C/W x 0.31) = 106.11W I_D = 106.11W/30V = 3.54A
So, @1ms pulse and 30V condition, suggested operating current will not be exceeding 3.54A.

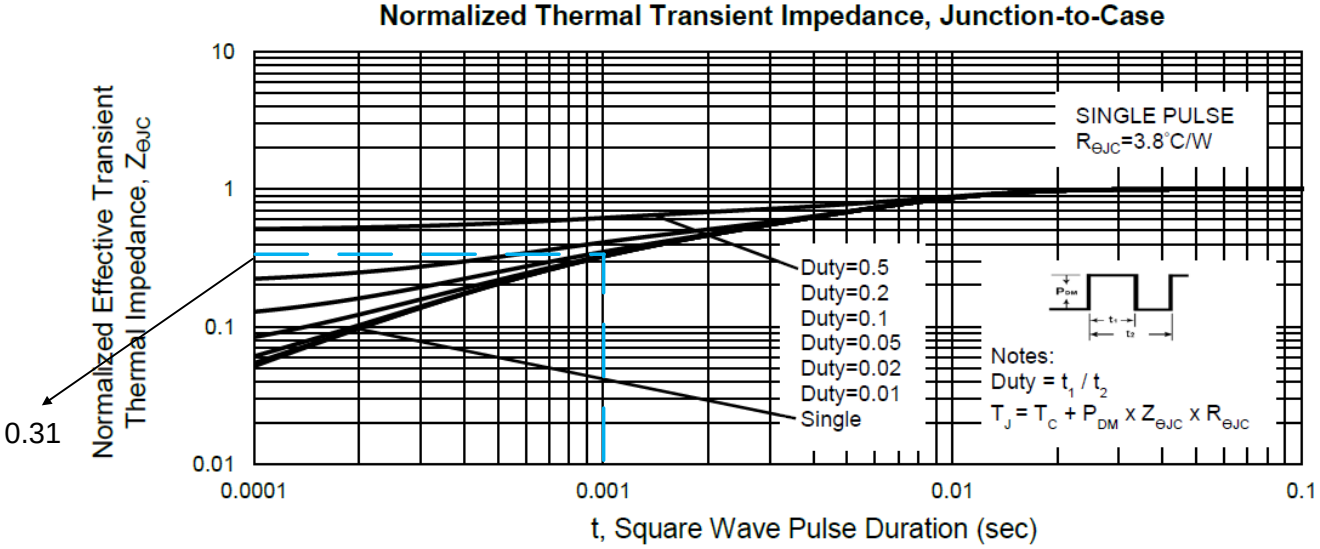
K is 1.85 @ 150°C - (Please refer to spec)
$R_{DS(on)}$ is 11.7mohm

$$I_D = \sqrt{\frac{T_J - T_C}{R_{\theta JC} \times K \times R_{ds(on)} \times Z_{\theta JC}}} \qquad V_{DS} = \frac{P_D}{I_D}$$

$$I_D = \sqrt{\frac{150^\circ C - 25^\circ C}{3.8^\circ C/W \times 0.31 \times 1.85 \times 11.7 mohm}} = 70.02A@1ms$$

V_{DS} = 106.11W / 70.02A = 1.515V (Corner voltage @1ms condition)

Normalized Thermal Transient Impedance, Junction-to-Case



Above picture provides the normalized effective transient thermal impedance. These curves can be Junction to Ambient or Case based. From above, TSC 30V MOSFET is based on junction to case condition. As the duty cycle and the pulse duration increase, the transient thermal impedance gets close to 1. In the other words, It approaches to steady state thermal resistance.

$$T_J = T_C + P_{DM} \times Z_{\theta JC} \times R_{\theta JC}$$

For example, the TSM120NA03CR run in single pulse condition, the $Z_{\theta JC}$ based on curve is 0.31 at 1ms. The $R_{\theta JC}$ is 3.8°C/W and P_{DM} is 1.5W. So the junction temperature of TSM120NA03CR at T_C=100°C can be got as below list.

T_J = 100°C + 1.5W x 0.31 x 3.8°C/W = 101.767°C

References

1. TSM120NA03CR ---------- 30V Power MOSFET Datasheet
2. Power FETs and their applications ----- Edwin S. Oxner
3. POWER MOSFETS Theory and Applications ----- Duncan A. Grant / John Gowar

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